

NANDrive™ Power Interrupt Data Protection

The Problem

The loss of data during a power fail event has been a concern for many memory technologies, particularly during program operations. Planar (2D) NAND flash memories, for example, have been vulnerable to “paired page” data corruption issues.

NAND flash is written in pages and a failed write to one page could lead to corruption of the data in its paired page. MLC NAND stores its two bits of data in one memory cell.

These two bits are in two different paired pages, which are programmed in separate stages because programming is done one page at a time. This means that if the power fails while writing to one page, the data in the paired page can also get corrupted. This type of error is difficult for a higher level file system (NTFS, XFS, Ext4, etc.) to handle because the host file system may have transaction failsafes in place, but it would have no idea that the paired page was affected. The data in the paired page may belong to a completely different file.

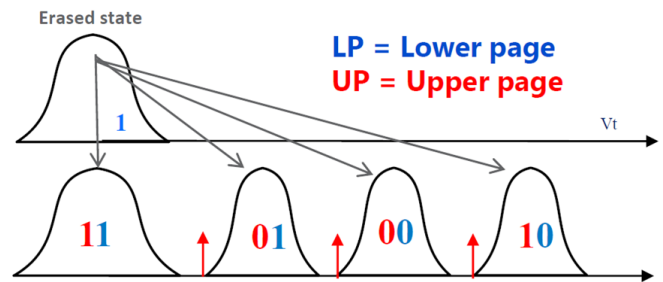
If this was a DLL or runtime file it could lead to a non-functional operating system or application on the drive. The contents of the paired page will contain uncorrectable (UNC) data where the charge state for some cells in the page is indeterminate and cannot be resolved to a 0 or 1.

The Solution

Traditional solutions to prevent this would involve retaining the power to the drive for sufficient time to allow the page program operation to complete. This could be achieved through on-board power hold-up capacitors to provide enough charge for the page program time, plus some program latency. If the drive being used had a DRAM cache, then the amount of stored energy would need to be significantly higher to prevent the cache contents from being lost.

Recent advances in memory architecture have enabled a new class of 3D NAND based solid state storage solutions that have eliminated the paired page issue. 3D NAND uses vertically stacked memory cell layers that can provide the same endurance as planar NAND flash with increased cost effectiveness and faster performance.

With Greenliant’s new industrial 3D MLC NAND based NANDrive™ devices, programming can now be achieved in a single pass where both pages are programmed at the same time. A representation of single-pass programming below shows the classic threshold voltage (V_t) distribution of cells in MLC NAND and how the charge state is decoded to the bit values for those cells.



Representation of single-pass programming

The upper and lower pages within a block can now be sequentially programmed by a NAND flash controller in one operation so the cell charge is moved to the required level for both pages simultaneously, effectively eliminating the possibility of data corruption in paired pages during power interrupts. Only the current page being written is at risk and this can be managed by a transaction failsafe host file system.

NANDrive™ Power Interrupt Data Protection

Advanced Features

With 3D MLC NAND's single-pass programming feature, the controller programs all states in a single step without disturbing adjacent cells and reducing the risk to data already in place on the drive (called "data at rest"). Furthermore, to retain data that could otherwise be lost due to program-and-erase errors, the controller may periodically update 3D NAND memory cells.

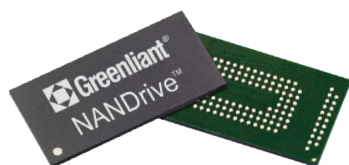
An intelligent controller, like those developed by Greenliant for use in its small form factor eMMC NANDrive and SATA NANDrive BGA SSDs, will help further minimize corruption of data in transition or in flight (in temporary DRAM or SRAM cache buffers) through use of advanced 3D NAND features. If the power fails

partway through the write operation, the host may typically use journaling or some other transaction failsafe protocol to determine that the last file written did not complete and therefore the data in that file should be ignored or replaced.

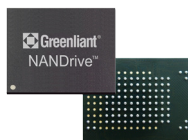
If the application uses small writes, which optimally should be the size of a NAND page, then sophisticated controller firmware will use advanced algorithms leveraging automatic read calibration to try to recover the last page, even if the power failed during the write operation. Controller adaptive threshold voltage tuning further enhances the ability of the controller to recover last page data.

Conclusion

These advances in controller and firmware design, coupled with new 3D NAND architectures, mean that there is no longer the requirement for hold-up capacitors and voltage detection circuitry to prevent drive corruption during a power failure. Greenliant's advanced BGA SSDs with built-in power fail data protection are designed to withstand unstable power environments and are ideal for high reliability applications.



SATA NANDrive
145-ball BGA






eMMC NANDrive
100-ball BGA



eMMC NANDrive
153-ball BGA

Greenliant SATA and eMMC NANDrive SSDs with Power Fail Data Protection

 twitter.com/Greenliant
 linkedin.com/company/Greenliant
 facebook.com/Greenliant

NANDrive FAQs: www.greenliant.com/nandrive-faqs

For more information, contact your Greenliant representative: www.greenliant.com/sales



© 2020 Greenliant
These specifications are subject to change without notice. 07/2020
Greenliant, the Greenliant logo and NANDrive are registered trademarks or trademarks of Greenliant.