Application Note
May 2010

INTRODUCTION

Like the GLS55LD019A, GLS55LD019B, GLS55LD019C, and GLS55LD019M, the GLS55LC200 is the heart of a high-performance, flash media-based data storage system with relatively minor differences. This application note describes the differences between the GLS55LC200 and the GLS55LC100/GLS55LC100M, and provides the guidelines to migrate current GLS55LC100/GLS55LC100M NAND flash controller based designs to a GLS55LC200 design.

This application note only covers the differences between these devices. For detailed product information, refer to the data sheets for each product.

Power Supply

The GLS55LC200 3V operating range has a lower minimum VDD/VDDQ voltage which results in a lower power consumption than the GLS55LC100/GLS55LC100M. The 5V operating range is the same for both GLS55LC200 and GLS55LC100/GLS55LC100M.

TABLE 1: Power Supply Differences

	GLS55LD019A/B/C/M	GLS55VD020
Power supply	3.135-3.465 V_{DD}/V_{DDQ}	2.7-3.465 V_{DD}/V_{DDQ}

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ATA/IDE Bus Interface Working Mode

The GLS55LC200 offers increased host interface data transfer rates as detailed below.

TABLE 2: ATA/IDE Bus Interface Working Mode Differences

	GLS55LD019A/B/C/M	GLS55VD020
Bus Width	8- or 16-bit access	16-bit access[1]
PIO Mode	Up to PIO mode 4	Up to PIO mode 6
Multi-word DMA	Up to Multi-word DMA mode 2	Up to multi-word DMA mode 4
Ultra DMA mode	Not supported	Up to Ultra DMA mode 4

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1. For 8-bit access, contact Greenliant for support and details.

NAND Flash Media Interface

TABLE 3: NAND Flash Media Interface Differences

	GLS55LD019A/B/C/M	GLS55VD020
Single Channel Mode[1]	Supported	Supported
Dual Channel Mode[2]	Not Supported	Supported
16-bit NAND Bus[3]	Supported	Not Supported
ECC	3 Random 12-bit Symbols Corrections	8 Random Bit Error Corrections
Single-level Cell Flash	Supported by GLS55LD019A/B/C	Supported
Multi-level Cell Flash	Supported by 55LD019M	Supported
Flash Page Size[4]	2 KBytes or 512 Bytes	2 KBytes and 4 KBytes

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1. In Single Channel Mode, for all devices, all NAND flash are connected with the low 8-bit data bus (FAD0:FAD7).
2. In Dual Channel Mode, for all devices, all NAND flash are connected evenly with the low 8-bit data bus (FAD0:FAD7), and with the high 8-bit data bus (FAD7:FAD15).

3. For GLS55LC100/GLS55LC100M, in 16-bit Access Mode, NAND flash with 16-bit data bus is connected with the 16-bit flash bus (FAD0:FAD15).
4. Dual Channel Mode can only be implemented when GLS55LC200 is interfacing with a 2 KByte page size NAND flash

Maximum Capacity and Performance

The maximum capacity of the GLS55LC200 is significantly larger than the GLS55LC100/GLS55LC100M, and the sustained Read and Write are faster.

TABLE 4: Maximum Capacity and Performance Differences

		GLS55LD019A/B/C/M	GLS55VD020
Maximum Capacity	Single Channel Mode	Up to 32 GBytes (with GLS55LD019C/M)	Up to 128 GBytes
	Dual Channel Mode	Not supported	UP TO 64 GBytes
Performance	Sustained Read	Up to 10 MBytes/sec	Up to 30 MBytes/sec
	Sustained Write	Up to 10 MBytes/sec	Up to 30 MBytes/sec

T4.0 2081

External Clock Interface

The external clock interface is not supported by the GLS55LC200. Because of this change, three pins of the GLS55LC200 have been re-defined.

TABLE 5: External Clock Differences

Pins			Functions	
TQFP (TQW)	**VFBGA (MVW)**	**TFBGA (BW)[1]**	**GLS55LD019A/B/C/M**	**GLS55VD020**
26	C9	J1	FCE7#/INTCLKEN	FCE7#
99	K9	A3	EXTCLKOUT	DNU
100	J8	B3	EXTCLKIN	TIE_DN

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1. The TFBGA (BW) package is not available for GLS55LC200.

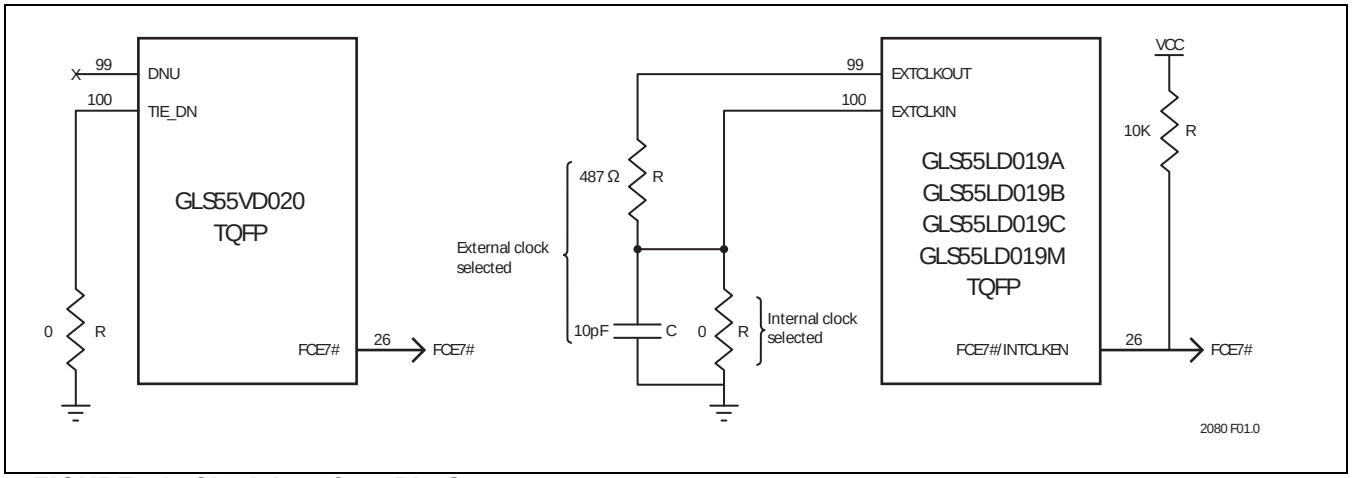

FIGURE 1: Clock Interface Pin Out

Pin Assignment

Both the GLS55LC200 and the GLS55LC100/GLS55LC100M are available in the 85-ball VFBGA and 100-lead TQFP packages. For these packages, the same printed circuit board (PCB) can be used when migrating from the GLS55LC100/GLS55LC100M to the GLS55LC200. For the most part, the pin assignments for both packages are the same between the GLS55LC200 and the GLS55LC100/GLS55LC100M. There are only six pins with different functions. See Table 6 for details.

TABLE 6: Pin Assignment Differences

Pins		Functions	
TQFP (TQW)	**VFBGA (MVW)**	**GLS55LD019A/B/C/M**	**GLS55VD020**
26	C9	FCE7#/INTCLKEN	FCE7#[1, 2]
62	D2	WP_PD#	IORDY
82	J3	FRDYbusy#	VREG
97	H7	FWP#	WP#/PD#
99	K9	EXTCLKOUT	DNU
100	J8	EXTCLKIN	TIE_DN

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1. The external clock interface, which is added to the FCE7# (pin 26) of the GLS55LC100/GLS55LC100M, is used to sense and slow down the system clock if an external clock mode is selected by the user. The GLS55LC200 does not support this feature.
2. On the GLS55LC200, FCE7# controls the direction of the external bus transceiver; FRE# controls the direction of the external bus transceiver on the GLS55LC100/GLS55LC100M.
   The FCE7# pin is firmware controlled. For GLS55LC200, when the FCE7# pin equals '1' it indicates the direction of write from controller-to-NAND; when the pin equals '0' it indicates the direction of read from NAND-to-controller.

Jumper resistors are required to make the PCBs compatible for either the GLS55LC100/GLS55LC100M or the GLS55LC200.

- Because the GLS55LC200 supports up to UDMA 4, termination resistors are necessary in the design.
- FAD0 and FAD7 are used to implement a single channel design for both the GLS55LC100/GLS55LC100M and the GLS55LC200.
- The GLS55LC200 does not support FWP# signals; therefore, WP# signals on NAND devices are pulled up when interfaced with the GLS55LC200.
- Add jumper resistors and capacitors to correspond with labels 019 or 020 in the design. for example, resistors and capacitors named 019 (i.e. R_019 and C_019) should be added in the GLS55LC100/GLS55LC100M

design. Resistors and capacitors named 020 (i.e. R_20 and C_20) should be added in the GLS55LC200 design.

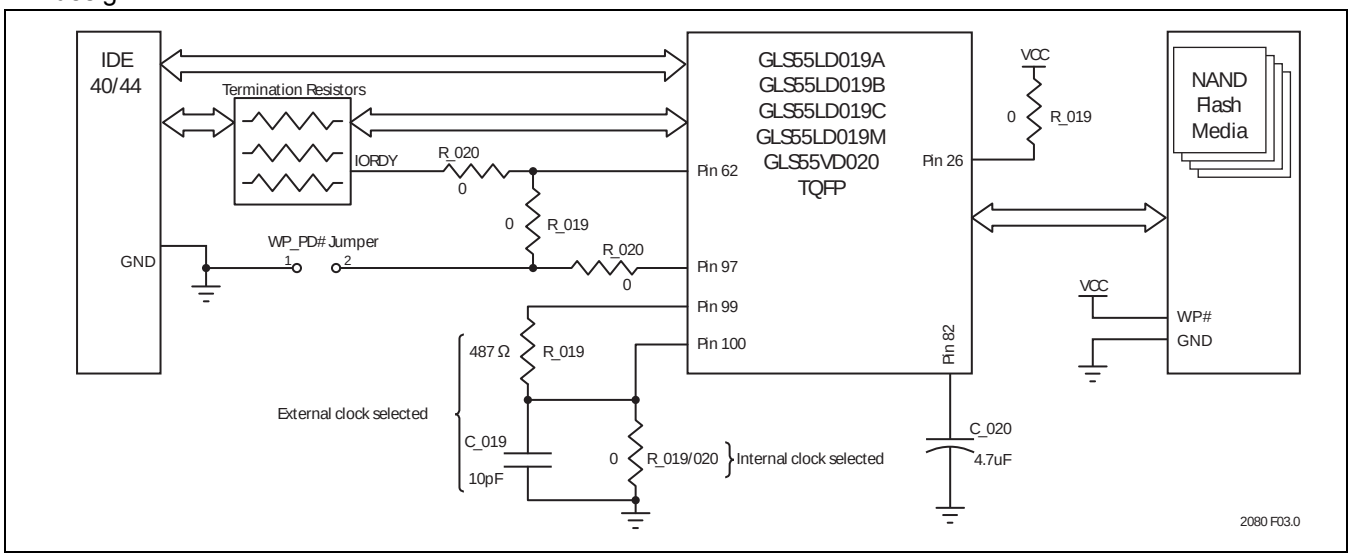

FIGURE 2: Design Modifications with Additional Jumper Resistors and Capacitors

Dual Channel Mode

The GLS55LC100/GLS55LC100M offers single channel 8-bit or 16-bit access interface for standard NAND flash media, while the GLS55LC200 supports single or dual channel 8-bit access.

TABLE 7: Single/Dual Channel Mode Differences

Product	Single-Channel	Dual-Channel	Functions
GLS55LD019A/B/C/M	Supported	Not Supported	Supports up to 8 flash media devices directly Supports up to 64 flash media devices with external decoding logic
GLS55VD020	Supported	Supported	Supports up to 4 flash media devices per channel Supports up to 8 flash media devices directly Supports up to 64 flash media devices with external decoding logic for single channel only—32 for dual channel.

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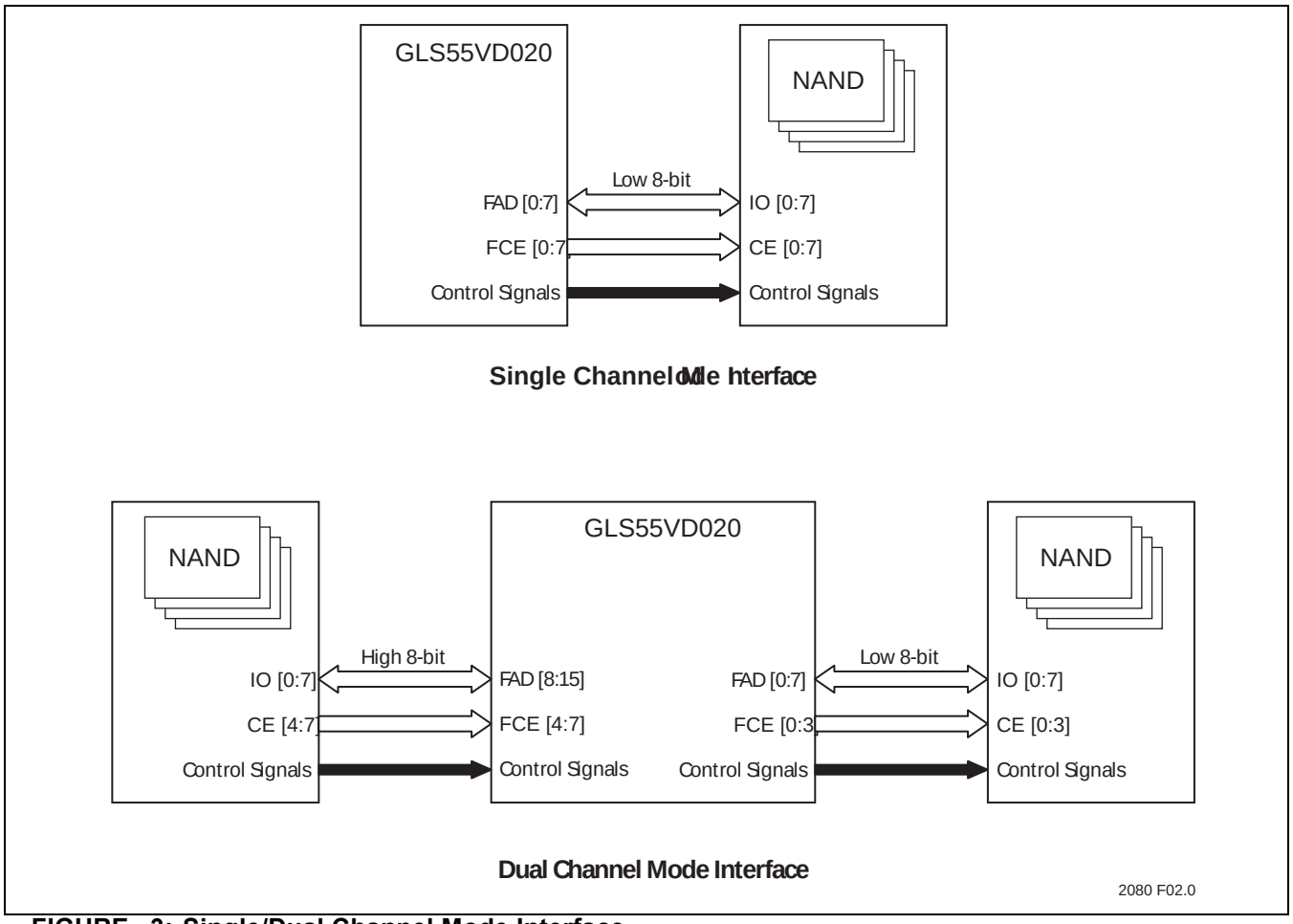

FIGURE 3: Single/Dual Channel Mode Interface

Note: Both GLS55LC100/GLS55LC100M and GLS55LC200 feature external decoding logic to attain maximum capacity. Refer to the reference design supplied by Greenliant for more information.
When not using the external decoding logic, FCE0# must be connected to CE of the NAND flash.

Application Note

Reference Designs and Tools

Reference designs and manufacturing tools are available to assist with your design needs. Many resources are also available on www.greenliant.com.

- Reference Designs: Contact your Greenliant sales representative for reference design schematics and a schematic review.
- Application Notes: Contact your Greenliant sales representative for available application notes.
- Tools: Contact your Greenliant sales representative for access to Manufacturing Utility, PT2 Windows version.

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